

REMARKS

Examiner's assistance during the May 5, 2005 telephone conference is greatly appreciated. The Examiner kindly agreed to reconsider the present application in view of Applicant's proposed amendment to claim 1 discussed during the telephone conference.

Claims 1, 3, 5, 7, 9, 11, 17, and 19 are presented for examination. Claim 1 has been amended to more clearly define the claimed invention over the prior art.

Claim 1, as amended, recites a cache memory system including a small-capacity cache memory which enables high-speed access and is provided between a processor and a main memory. The cache memory system comprises:

- a software cache controller which performs software control for controlling data transfer to the cache memory in accordance with a preliminarily programmed software; and

- a hardware cache controller which performs hardware control for controlling data transfer to the cache memory by using a predetermined hardware.

The claim specifies that:

- the processor causes the software cache controller to perform the software control but causes the hardware cache controller to perform the hardware control when it becomes impossible to perform the software control, and

- when a cache miss happens at the time of the software control, the processor automatically causes the hardware cache controller to perform the hardware control.

Further, the claim was amended to more clearly indicate that the hardware cache controller performs line management of the cache memory by using a set-associative method for multiple ways, and the software cache controller performs line management of the cache memory by using a fully associative method for at least one way in the multiple ways and by using the set-associative method for at least another one way of said multiple ways.

Hence, the claim specifically indicates that the software cache controller performs line management of the cache memory not only by using a fully associative method for at least one way of the multiple ways, but also by using the set-associative method for at least another one way of the multiple ways.

It is noted that claims 1, 3, 5, 9, 17 and 19 stand rejected under 35 U.S.C. 103 as being unpatentable over the Fujiwara publication in view of the Hallnor publication.

The previous Office Action admits that the Fujiwara publication does not disclose the claimed line management performed by the hardware and software cache controllers. However, the Office Action relies upon the Hallnor publication (Section 2, paragraphs 1, 3 and 4) for disclosing that “hardware controlled management is better suited for a low-associativity cache (i.e. multi-way set-associative)...., and software controlled management is better for fully-associative cache.”

Considering Hallnor, the reference discloses that in some areas, a fully-associative software managed secondary cache offers an advantage over low-associativity, hardware-managed organizations.

However, the reference does not suggest hardware management that uses a set-associative method for multiple ways, and the software management that uses a fully associative method for at least one way of these multiple ways and the set-associative method for at least another one way of these multiple ways, as the amended claim 1 requires.

Support for the present amendment of claim 1 may be found in the specification, for example, on page 9, lines 13-21.

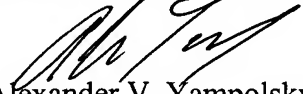
In view of the foregoing, and in summary, claims 1, 3, 5, 7, 9, 11, 17, and 19 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

Application No.: 10/076,625

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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